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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/624,625	07/22/2003	Anthony J. Benson	200300217-1	6588

22879 7590 07/18/2006

HEWLETT PACKARD COMPANY
P O BOX 272400, 3404 E. HARMONY ROAD
INTELLECTUAL PROPERTY ADMINISTRATION
FORT COLLINS, CO 80527-2400

EXAMINER	
PARK, ILWOO	

ART UNIT	PAPER NUMBER
2182	

DATE MAILED: 07/18/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/624,625	BENSON ET AL.	
	Examiner	Art Unit	
	Ilwoo Park	2182	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 April 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-16* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Following rejections now apply in response to the amendment filed on 4/28/2006. claims 1-16 are presented for examination.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1 and 5 are rejected under 35 U.S.C. 102(e) as being anticipated by Bicknel et al. [US 2003/0193776 A1].

As for claim 1, Bicknel et al teach an apparatus comprising:

input/output (I/O) controller circuit boards [controller 108.1 and 108.2 in figs 1 and 7];

a storage array circuit board [e.g., intermediate electronic component 110 in fig. 6 or midplane card 112 in fig. 7] having storage device connectors to couple storage devices [disk drive 106.1-106.4] to the storage array circuit board; and

a signal routing circuit board [e.g., midplane card 112 in fig. 7 or intermediate electronic component 110 in fig. 6] having one or more connectors to couple the storage array circuit board to the signal routing circuit board, connectors to couple I/O controller circuit boards to the signal routing circuit board, and one or more multiplexers [MUX

208] to route data signals in a selective manner along one or more first data signal paths [e.g., ref. No. 206 from controller 108.1] between a first I/O controller circuit board and the storage array circuit board and along one or more second data signal paths [e.g., ref. No. 206 from controller 108.1] between a second I/O controller circuit board and the storage array circuit board, wherein the second data signal path(s) share a portion [e.g., path between MUX 208 and disk drive 106 in fig. 7] of one or more data signal paths of the first data signal path(s).

4. As for claim 5, Bicknel et al teach the signal routing circuit board defines one or more shared control signal paths to route power control and/or status signals between the storage array circuit board and one or more I/O controller circuit boards [figs. 6-8; paragraph 0031].

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 3, 4, 6-9 and 13-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bicknel et al. [US 2003/0193776 A1] in view of Felton et al. [US 2004/0193791 A1].

As for claim 7, Bicknel et al teach a storage system comprising:

a housing [e.g., fig. 1];

a storage array circuit board [e.g., intermediate electronic component 110 in fig. 6 or midplane card 112 in fig. 7] for mounting in the housing, the storage array circuit board having a plurality of storage device connectors for removably coupling a plurality of storage devices to the storage array circuit board;

at least one input/output (I/O) controller circuit board [controller 108.1 and 108.2 in figs 1 and 7] for insertion in the housing, each I/O controller circuit board for communicating with storage devices; and

a signal routing circuit board [e.g., midplane card 112 in fig. 7 or intermediate electronic component 110 in figs. 5 and 6] for removable connection to the storage array circuit board and with each I/O controller circuit board.

Though Bicknel et al disclose electronics [e.g., fans, power supplies, and other components in paragraph 0017] common to circuit boards, Bicknel et al do not expressly disclose the signal routing circuit board having the electronics connected thereto and removable from the housing without removal of the storage array circuit board. Felton et al teach a signal routing circuit board [e.g., midplane 208 in fig. 7] having electronics [e.g., power supply 112 in fig. 8] common to circuit boards connected thereto, the signal routing circuit board for removable connection to a storage array circuit board [e.g., adapter board 216 in fig. 5] and with each I/O controller circuit board [link control card 108 in fig. 2], wherein the electronics are removable from a housing without [paragraph 0024] removal of the storage array circuit board. At the time of the invention, one of ordinary skill in the art would have been motivated to modify the cited

combination of references in order to increase conveniency by providing connectors to the signal routing circuit board for the electronics common to circuit boards.

7. As for claim 8, Bicknel et al teach the signal routing circuit board has one or more multiplexers [MUX 208] to route data signals in a selective manner along one or more first data signal paths [e.g., ref. No. 206 from controller 108.1] between a first I/O controller circuit board and the storage array circuit board and along one or more second data signal paths [e.g., ref. No. 206 from controller 108.1] between a second I/O controller circuit board and the storage array circuit board, and wherein the second data signal path(s) share a portion [e.g., path between MUX 208 and disk drive 106 in fig. 7] of one or more data signal paths of the first data signal path(s).

8. As for claim 9, Felton et al teach the signal routing circuit board is positioned in a generally orthogonal orientation relative to the storage array circuit board when connected to the storage array circuit board [figs. 3A and 7].

9. As for claims 3 and 13, Bicknel et al and Felton et al teach one or more power supplies for insertion in the housing and removable coupling to the storage array circuit board or the signal routing circuit board defining one or more paths to supply power from the storage array circuit board to one or more I/O controller boards [implicit: paragraph 0017 and fig. 1 of Bicknel et al].

10. As for claims 4 and 14, Bicknel et al teach the signal routing circuit board [either one or midplane 112 or intermediate electronic component 110 as shown in figs. 6 and 7] and Felton et al teach one or more voltage regulators [on a board away from a board

of direct connection to the power supply in figs. 4 and 7] to supply power at one or more levels to at least one I/O controller circuit board.

11. As for claim 15, Bicknel et al teach the signal routing circuit board defines one or more shared control signal paths to route power control and/or status signals between the storage array circuit board and at least one I/O controller circuit board [figs. 6 and 8].

12. As for claims 6 and 16, Felton et al teach the signal routing circuit board defines one or more signal paths to route signals between I/O controller circuit boards [e.g., signal line 244 in fig.2].

13. Claims 2, 7-9, 11, 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bicknel et al. [US 2003/0193776 A1] in view of Manweiler et al. [US 6,208,522 B1].

As for claim 7, Bicknel et al teach a storage system comprising:

a housing [e.g., fig. 1];

a storage array circuit board [e.g., intermediate electronic component 110 in fig. 6 or midplane card 112 in fig. 7] for mounting in the housing, the storage array circuit board having a plurality of storage device connectors for removably coupling a plurality of storage devices to the storage array circuit board;

at least one input/output (I/O) controller circuit board [controller 108.1 and 108.2 in figs 1 and 7] for insertion in the housing, each I/O controller circuit board for communicating with storage devices; and

a signal routing circuit board [e.g., midplane card 112 in fig. 7 or intermediate electronic component 110 in figs. 5 and 6] for removable connection to the storage array circuit board and with each I/O controller circuit board.

Bicknel et al do not expressly disclose the signal routing circuit board having the electronics common to circuit boards connected thereto and removable from the housing without removal of the storage array circuit board. Manweiler et al teach a signal routing circuit board [midplane 76 in figs. 9-12] having electronics [e.g., removable processor module 16 in fig. 1] common to circuit boards connected thereto, the signal routing circuit board for removable connection to a storage array circuit board [e.g., media drive module 18 in figs. 1 and 6] and with each I/O controller circuit board [e.g., I/O module 36 in figs. 2 and 8], wherein the electronics are removable from a housing without removal of the storage array circuit board. At the time of the invention, one of ordinary skill in the art would have been motivated to modify the cited combination of references in order to increase modularity for the circuit boards [Manweiler et al: col. 1, lines 60-67].

14. As for claim 8, Bicknel et al teach the signal routing circuit board has one or more multiplexers [MUX 208] to route data signals in a selective manner along one or more first data signal paths [e.g., ref. No. 206 from controller 108.1] between a first I/O controller circuit board and the storage array circuit board and along one or more second data signal paths [e.g., ref. No. 206 from controller 108.1] between a second I/O controller circuit board and the storage array circuit board, and wherein the second data signal path(s) share a portion [e.g., path between MUX 208 and disk drive 106 in fig. 7] of one or more data signal paths of the first data signal path(s).

15. As for claim 9, Manweiler et al teach the signal routing circuit board is positioned in a generally orthogonal orientation relative to the storage array circuit board when connected to the storage array circuit board [figs. 1 and 3].

16. As for claim 11, Manweiler et al teach a housing defines an opening [col. 4, lines 17-22] in a side for insertion of the signal routing circuit board in the housing and an opening in an end for insertion of at least one I/O controller circuit board [I/O module 36 in figs. 2 and 8].

17. As for claims 2 and 12, Manweiler et al teach a system circuit board [removable processor module 16] for removable connection to a signal routing circuit board [midplane 76 in figs. 9-12].

18. Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Bicknel et al and Felton et al as applied to claim 7 above, and further in view of Barringer et al. [US 2004/0062002 A1].

As for claim 10, Bicknel et al and Felton et al do not disclose at least one I/O controller circuit board is positioned in a generally planar orientation relative to the signal routing circuit board when connected to the signal routing circuit board. Barringer et al teach at least one I/O controller circuit board [planar boards 14A, 14B arranged in side-by-side in figs. 1 and 6] is positioned in a generally planar orientation relative to a signal routing circuit board [midplane 28 in figs. 1 and 6] when connected to the signal routing circuit board. At the time of the invention, one of ordinary skill in the art would have been motivated to modify the cited combination of references in order to increase flexibility in packaging of a housing.

Response to Arguments

19. Applicant's arguments, see page 3, filed 4/28/2006, with respect to claims 1-16 have been fully considered and are persuasive. The rejection of claims 1-16 has been withdrawn.

Conclusion

20. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ilwoo Park whose telephone number is (571) 272-4155. The examiner can normally be reached on Monday through Friday from 9:00 AM to 5:30 PM. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kim Huynh can be reached on (571) 272-4147. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

ILWOO PARK
PRIMARY EXAMINER

Ilwoo Park
July 10, 2006